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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/099,707	03/13/2002	Stjepan W. Andrasic	174/223	2004

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/099,707	ANDRASIC ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-26* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 19-20 and 23-24 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In this instant, claim 19 calls for a voltage controlled oscillator circuitry comprises the programmable differential delay cells of claim 18 rather than further limit the subject matter of the programmable differential delay cells of claim 18.

2. Similarly, claim 20 calls a phase locked loop circuitry comprises the programmable differential delay cells of claim 18 rather than to further limit the subject matter of programmable differential delay cells of claim 18.

3. Claims 23 and 24 are also objected for the same reasons as noted above.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-5, 7-12 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Huizer (USP 5,477,182). Figure 3 of Huizer shows a differential delay cell comprising a plurality of load transistors (cl1, l1) connectable in parallel with one another, a plurality of bias current transistors (S) connectable in parallel with one another, a switching transistor (N1),

switching circuitry (not show) producing control voltage (c1, c2, c1/ and c2/) to selectively operatively connect at least one of the load transistors in parallel with at least one other of the load resistance transistors as called for in claims 1, 7-12 and 17-19.

Regarding claims 3 and 15, a plurality of further load resistance transistors are seen as l2 and cl2 of Huizer's figure 3, a further switching transistor is seen as transistor N2 of Huizer's figure 3, I and ib are complementary input signals.

Regarding claims 4 and 16, the further load resistance transistors are controlled by the switching circuitry (not shown) which producing control voltages c1, c2, c1/ and c2/.

Regarding claim 5, the switching circuitry (not shown) is programmable to generate the desired control voltages c1, c2, c1/ and c2/.

Claims 1-22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshihiro (EP 987822A2), prior art cited on PTOL-1449. Figure 7 of Yoshihiro shows a differential delay cell comprising a plurality of load transistors (750, 755) connectable in parallel with one another, a plurality of bias current transistors (754, 757) connectable in parallel with one another, a switching transistor (752), switching circuitry (not show) producing control voltage (707) to selectively operatively connect at least one of the load transistors in parallel with at least one other of the load resistance transistors as called for in claims 1, 7-12, 17-22 and 24.

Regarding claim 2, further switching circuitry (not shown) producing control voltage (708) to selectively operatively connect at least one of the bias current transistors in parallel with at least one other of the bias current transistors.

Regarding claims 3 and 15, a plurality of further load resistance transistors are seen as

transistors 751 and 756 of Yoshihiro's figure 7, a further switching transistor is seen as transistor 753 of Yoshihiro's figure 7, signals 702 and 703 are complementary input signals.

Regarding claims 4 and 16, the further load resistance transistors are controlled by the switching circuitry (not shown) which producing control voltage 707.

Regarding claims 5-6, the switching circuitry (not shown) is programmable to generate the desired control voltage 707.

Regarding claims 13-14, the enablement of the bias current transistors are seen by the turn on/off the transistor 757 of Yoshihiro's figure 7.

Regarding claims 20-22 and 24, the voltage controlled oscillator 30 of Yoshihiro's figure 6 is used in a phase locked loop as shown in figure 4 of Yoshihiro.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshihiro (EP 987,822). Yoshihiro discloses all the aspects of the present invention as noted above except for coupling the programmable logic device to a processor and a memory device in a digital processing system as called for in claim 23. However, it is notoriously well known in the art that digital processing system, i.e., microcomputer, commonly consisting of a processor, a memory and programmable logic device (clock generator) coupled to the processor and the memory to insure a synchronous operation in transferring data in or out to or from the components.

Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the programmable logic device in a digital processing system to provide a synchronous operation between components thus ensuring erroneous free operative device.

Regarding claim 24, since an integrated circuit manufactured by mass production is readily available and inexpensive, one skilled in the art would have been taken to realize mounting the integrated circuit on a printed circuit board to minimize the cost of producing. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to mount the integrated programmable logic device on a printed circuit board for the purpose of minimizing cost of producing.

8. Regarding claims 25-26, Yoshihiro discloses all the aspects of the present invention as noted above except for coupling the programmable logic device to a processor and a memory device in a digital processing system as called for in claims 25-26. However, it is notoriously well known in the art that digital processing system, i.e., microcomputer, commonly consisting of a processor, a memory and programmable logic device (clock generator) coupled to the processor and the memory to insure a synchronous operation in transferring data in or out to or from the components. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the programmable logic device in a digital processing system to provide a synchronous operation between components thus ensuring erroneous free operative device.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 730-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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March 12, 2003